Pin Descriptions

PIN NAME	PIN NUMBER ES1020QI	DESCRIPTION
V_{DD}	23	Chip Bias. Bias IC from nominal 1.5V to 5V.
GND	10	Bias Return. IC ground.
$\overline{\text{ENABLE}}$_1	1	Input to start on/off sequencing. Input to initiate start of programmed sequencing of supplies on or off. Enable functionality disabled for 10ms after UVLO is satisfied.
$\overline{\text{RESET}}$	24	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ provides low signal 150ms after all GATEs are fully enhanced. Delay is for stabilization of output voltages. $\overline{\text{RESET}}$ asserts low upon UVLO not being satisfied or $\overline{\text{ENABLE}}$ being deasserted. $\overline{\text{RESET}}$ outputs are open-drain, N-channel FET and are guaranteed to be in correct state for VDD down to 1V and are filtered to ignore fast transients on VDD and UVLO_X.
UVLO_A	20	Undervoltage Lockout/Monitoring Input. Provides a programmable UV lockout referenced to an internal 0.633V reference. Filtered to ignore short (<30µs) transients below programmed UVLO level.
UVLO_B	12	
UVLO_C	17	
UVLO_D	14	
DLY_ON_A	21	Gate On Delay Timer Output. Allows programming of delay and sequence for VOUT turn-on using a capacitor to ground. Each capacitor charged with 1µA 10ms after turn-on initiated by $\overline{\text{ENABLE}}$. Internal current source provides delay to associated FET GATE turn-on.
DLY_ON_B	8	
DLY_ON_C	16	
DLY_ON_D	15	
DLY_OFF_A	18	Gate Off Delay Timer Output. Allows programming of delay and sequence for VOUT turn-off through $\overline{\text{ENABLE}}$ via a capacitor to ground. Each capacitor charged with 1µA internal current source to an internal reference voltage, causing corresponding gate to be pulled down, thus turning off FET.
DLY_OFF_B	13	
DLY_OFF_C	3	
DLY_OFF_D	4	
GATE_A	2	FET Gate Drive Output. Drives external FETs with 1µA current source to soft-start ramp into load.
GATE_B	5	
GATE_C	6	
GATE_D	7	
$\overline{\text{SYSRST}}$	22	System Reset I/O. As an input, allows for immediate and unconditional latch-off of all GATE outputs when driven low. This input can also be used to initiate programmed sequence with ‘zero’ wait (no 10ms stabilization delay) from input signal on this pin being driven high to first GATE. As an output, when there is a UV condition, this pin pulls low. If common to other $\overline{\text{SYSRST}}$ pins in a multiple IC configuration, it causes immediate and unconditional latch-off of all other GATEs on all other ES1020QI sequencers.
GND	EPAD	Ground. Die Substrate. Can be left floating.
NC	9, 11, 19	No Connect